

IN THE CLAIMS:

Please amend claims 1-4 as shown in the complete list of claims that is presented below.

1. (currently amended) A layout of a flash memory having symmetric select transistors, comprising:
 - a memory cell array;
 - a polysilicon gates extending in a direction perpendicular to the memory cell array and cooperating with a plurality of pairs of sources/drains ~~arranged at two sides thereof~~ for forming a plurality of select transistors; and
 - a wires connecting the plurality of select transistors and the memory cell array.
2. (currently amended) The layout according to claim 1, wherein the wires comprises a segments parallel to the polysilicon gates.
3. (currently amended) A layout of a flash memory having symmetric select transistors, comprising:
 - a memory cell array; and
 - a polysilicon gates corresponding to a plurality of select transistors extending in a direction perpendicular to the memory cell array; wherein the plurality of select transistors are arranged substantially symmetric with respect to the memory cell array.
4. (currently amended) The layout according to claim 3, further comprising a metal wires extending from the memory cell array toward the polysilicon gates for connecting the plurality of select transistors to ~~a bit line of~~ the memory cell array.